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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/805,199	03/14/2001	Masaki Wakabayashi	1248-0537P-SP	1722

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EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/805,199	WAKABAYASHI ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 1, 2006 has been entered.

Response to Amendment

2. This Office Action is in response to applicant's communication filed May 1, 2006 in response to PTO Office Action mailed April 11, 2006. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

3. In response to the last Office Action, claims 1 and 17 have been amended. No claims have been canceled. No claims have been added. As a result, claims 1-22 remain pending in this application.

Response to Arguments

4. Applicant's arguments filed May 1, 2006 have been fully considered but they are not persuasive. As to the Remarks, Applicant asserted that:

(a) The Examiner's rejection is contradictory because Applicant cannot ascertain whether or not the Examiner is contending that Rabeler does or does not teach a monitor flag.

Examiner would like to point out that Rabeler does disclose a monitor flag, when Rabeler discloses a mode bit that toggles between a system mode and a user mode (see column 1, lines 31-41). However, Rabeler does not specifically teach a monitor flag that indicates that a specified address space is being accessed as pointed out in page 3 of the office Action. Bournas has been cited to cure this deficiency.

(b) Bournas does not suggest toggling a flag indicating that a predetermined address space is being accessed.

Examiner respectfully traverses. Bournas discloses a flip-flop, which can be set to different state, based on a value situated in an addressing space and which supplies a locking/unlocking signal for inhibiting access (see column 4, lines 5-35 and column 6, lines 38-60). Thus, it can be clearly seen that Bournas indicates that an address space is being accessed by monitoring the state of a flip-flop in the same manner claimed by applicant.

(c) Sasaki does not teach or suggest does nor suggest "determining whether a writing operation occurs from a predetermined address space or from an address space other than the predetermined address space".

Examiner respectfully traverses. Sasaki discloses the above limitation when Sasaki teaches, "when program B has accessed an address space other than the enable addresses invalidly (see column 7, lines 35-53). Thus, it can be clearly seen that Sasaki teaches determining access to two different address spaces in the same manner claimed by applicant.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-7, 10-15 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabeler (US 6,594,746) and Bandoo (US 3,803,559) and Bournas (US 5,452,431).

As in claim 2, Rabeler discloses a system comprising:

an access permission address range setting register operable to set, when said flag is toggled, an address range within which an access is permitted (column 1 line 66 to column 2, line 144 Fig. 3, element 32; column 4, lines 54-65);

a judging means for judging whether or not an access is carried out within the address range set during execution of software (i.e. a user program) (Fig. 3; column 4, lines 47-65); and control means for controlling an access with respect to a memory based on a result of the judging means (Fig. 3., column 4, lines 47-65).

Rabeler does not teach a monitor flag for indicating that a specified address space is being accessed; and an access permission setting register for setting whether or not an access with respect to an address other than the address range should be permitted, that is able to be set while the flag is set, nor does Rabeler teach that the memory access is controlled based on the content of the access permission setting access register as required by claim 2.

Rabeler also does not teach an interruption request signal generating means for generating an interrupt to a processing unit when accessing an address other than the address range while the access permission register is set so as not to permit access to an address outside the address range, whereupon a predetermined interrupt program is executed as required by claim 4.

Bandoo teaches a system for inhibiting memory access based on an address range, comprising a protect check flip-flop (i.e. access permission setting register) that sets whether or not an access with the respect to an address other than the address range should be permitted, by overriding the result of an address range judging means

such that memory access is controlled based on a result of the judging means and the content set by the access permission setting register (Fig. 3; column 3, line 57 to column 4, line 7). Bandoo teaches that by this mechanism, a supervisory program may be allowed to conveniently access all memory areas (Column 4, lines 45-57). Bandoo further teaches indicating that a specified address space is being accessed (Column 2, lines 14-42)

Regarding claim 2, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to incorporate the access permission setting register mechanism of Bandoo, in the system of Rabeler, in order to allow convenient access to all memory areas by a supervisory program as taught by Bandoo.

Still Regarding claim 2, Rabeler and Bandoo do not teach indicating that a predetermined address space is being accessed, based on an address bus signal and an instruction read out signal indicative of a first cycle of an instruction as required in the claim.

Bournas teaches a microcircuit for a chip card wherein an indication that a predetermined address space is being accessed is based on an address bus signal and an instruction read out signal indicative of a first cycle of an instruction (column 6, lines 38-60).

Regarding claim 2, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to incorporate an indication that a predetermined address space is being accessed is based on an address bus signal and an instruction read out signal indicative of a first cycle of an instruction of Bournas, in the system of Rabeler and Bandoo, in order to maintain high security level in the chip card (column 2, lines 32-34) as taught by Bournas.

Further regarding claim 2, because Rabeler teaches that all memory access inhibition registers can only be modified in system mode (i.e. when the monitor flag is set) (Column 1, lines 31-41; Column 2, lines 32-34), it would have been obvious to only allow modification of the access permission setting register while in system mode.

Claim 3 is rejected using the same rationale as for the rejection of claim 2, further noting that Rabeler teaches a system program for setting all registers associated with inhibition of memory access (Column 1, lines 40-43) column 2, lines 32-34), where it is readily apparent that the system program must be executed prior to the user program in order for the security relevant information to be effective, and that the user program executes subsequent to the system Program.

Bandoo further teaches a generating means for generating an interrupt to the processing system when access to an address other than the permitted address range while the protect check flip-flop (i.e. access permission register) is set so œs not to

permit access to an address outside the address range, whereupon an interrupt handling routine of the supervisory program is executed (Fig. 4) column 5, lines 13-34).

Bandoo teaches that this may be used to inform an operator of the condition (column 5, line 34).

Regarding claim 4, it would have been obvious to one or ordinary skill in the art at the time of invention by applicant, to use the interrupt mechanism of Bandoo, in the system of Rabeler, in order to notify an operator of an attempted access to an address outside the address range as taught by Bandoo.

Claim 5 is rejected using the same rationale as for the rejection of claim 4 above.

Claim 6 is rejected using the same rationale as for the rejection of claim 4, noting that Bandoo teaches the interrupt handling routine is part of the supervisory program (Column 5, lines 20-24).

Claim 7 is rejected using the same rationale as for the rejection of claim 6 above.

Claims 10-15 are rejected using the same rationale as for the rejection of claims 2-7 respectively, where it is noted that Rabeler teaches that the memory comprises a rewritable non-volatile memory (column 3, lines 7-19).

Claim 18 is rejected using the same rationale as for the rejection of claim 2 above.

Claim 19 is rejected using the same rationale as for the rejection of claim 3 above.

Claim 20 is rejected using the same rationale as for the rejection of claim 4 above.

Claim 21 is rejected using the same rationale as for the rejection of claim 6 above.

7. Claims 1, 9 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabeler (US 6,594,746) and Bandoo (US 3,803,559) and Sakaki (EP 0,735,488).

Claim 1 is rejected using the same rationale as for the rejection of claim 2 above. However, Rabeler and Bandoo does not teach "a register writing control means for determining whether a writing operation occurs in a predetermined address space or in an address space other than the predetermined address space and outputting a writing reference signal when the writing operation occurs in the predetermined address space" and "an access permission address range setting means for setting an address range

within which access by the application program to be executed is permitted only when the writing reference signal is output" as recited in the claim.

Sakaki discloses a register writing control means for determining whether a writing operation occurs in a predetermined address space or in an address space other than the predetermined address space and outputting a writing reference signal when the writing operation occurs in the predetermined address space (column 2, lines 19-45); and an access permission address range setting means for setting an address range within which access by the application program to be executed is permitted only when the writing reference signal is output (column 2, line 58 – column 3, line 16; column 7, lines 5-29).

Regarding claim 1, it would have been obvious to one or ordinary skill in the art at the time of invention by applicant, to use a register writing control means and an access permission address range setting means of Sakaki, in the system of Rabeler and Bandoo, in order to provide an improved execution controlling for a one-chip microcomputer that inhibits a program from unnecessarily accessing another program in executing programs but also increases the security of the programs and data (column 2, lines 11-18) as taught by Sakaki.

Claim 9 is rejected using the same rationale as for the rejection of claim 1, where it is noted that Rabeler teaches that the memory comprises a rewritable non-volatile memory (column 3, lines 7-19).

Claim 17 is rejected using the same rationale as for the rejection of claim 1 above.

8. Claims 8, 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabeler (US 6,594,746) in view of Bandoo (US 3,803,559) and Bournas (US 5,452,431) as applied to claims 3 and 19 above, and further in view of Oppenheimer (David L. Oppenheimer et al, "Performance Signatures: A Mechanism for Intrusion Detection", 1997 Information Survivability Workshop - ISW'97).

Rabeler and Bandoo and Bournas are relied upon for the teachings relative to claims 3 and 19 as above.

The combination of Rabeler and Bandoo and Bournas does not teach a re-execution forbidding means for storing information indicating that an access is carried out beyond an access limit, wherein the control means controls the memory based on the information so that access is not carried out again beyond the access limit as required by claim 8.

Oppenheimer teaches a general principle for survivability in a computer system subject to anomalous program behavior, where software components that are misbehaving are quarantined (i.e. prevented from re-executing) (Introduction, paragraph 1, lines 1-3). Oppenheimer defines one kind of anomalous behavior as a memory usage being outside a normal range (Section 1, paragraph 2, lines 1-9; Section 2. 1, lines 1-11).

Although Oppenheimer teaches anomalous program behavior in the context of a hostile attack, to one skilled in the art Oppenheimer's teachings would suggest general principles applicable to any anomalous program behavior. Furthermore, it is readily apparent in Oppenheimer that an indication of anomalous behavior must be stored in order for the system to make reference to the condition during analysis of the anomalous behavior (Section 2.2).

Regarding claim 8, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to prevent a program from re-executing (i.e. quarantine) based on information stored indicating anomalous memory usage as taught by Oppenheimer, in the system made obvious by the combination of Rabeler and Bandoo, where the anomalous behavior is an access beyond an access limit, in order to ensure survivability of the computer system against misbehaving software as taught by Oppenheimer.

Claim 16 is rejected using the same rationale as for the rejection of claim 11 above.

Claim 22 is rejected using the same rationale as for the rejection of claim 8 above.

Conclusion

9. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

10. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (571) 272-4215. The examiner can normally be reached on 8:30 am - 6:00 pm, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 27, 2006

PIERRE VITAL
PRIMARY EXAMINER